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VHDL & FPGA Implementation of Max Membership Principle Based on Defuzzifier Unit

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Abstract :

the fuzzy data that obtained from the fuzzification process is not appropriate for the real time applications and have to be converted into crisp form. The conversion of data from fuzzy form to crisp form is known as the defuzzification, also called as "rounding off". This paper proposes VLSI architecture of a Max Membership Principle (MMP) defuzzification method. The MMP of defuzzification is simple and is being generally used in comparison to more complex weighted average defuzzification method. The proposed architecture has been modeled in VHDL and implemented in XILINX and Spartan - 3 field programmable gate arrays (FPGA). It is more efficient in the area and the speed of operation in comparison to a more complex architecture used for the weighted average method. The functional analysis has revealed that the proposed architecture is implementing MMP based defuzzifier efficiently and accurately.

Keywords : Defuzzification; Fuzzy processor; Max Membership Principle; Low power; VLSI design .

I. Introduction

The modern concept of fuzzy sets was introduced by Lotfi Zadeh [1-2] in his work "Fuzzy Sets" which described the mathematics of fuzzy set theory nearly three decades ago. Although a relatively new theory, fuzzy logic has been used in many engineering applications because being considered as a simplistic solution available for the specific problems. Fuzzy systems have high potential to understand the systems that are devoid of analytic formulations: complex systems [3-7].

In this work, a novel VLSI architecture of a defuzzifier has been proposed. It has been modeled in VHDL and

implemented in Spartan-3 FPGA. The defuzzifier designed is based on the max membership principle (MMP) defuzzification. Mostly, weighted average method has been used for defuzzification and VLSI architectures for weighted average defuzzification has been designed and developed many times. Since weighted average method cannot be used for max membership functions [8-10], Sajad A. Loan et al [11, 12] has developed a Center of Gravity and Weighted average method Defuzzification architecture for fuzzy processors respectively, Asim M. Murshid [13-15] has developed Mean Max and Center of Sums Defuzzification architecture for fuzzy processors and Multi Membership Function respectively. Therefore, the MMP method is being used first time to our knowledge. Further, MMP method is the most prevalent and physically appealing of all the defuzzification methods. In this work, a model has been developed from which the defuzzified value has been obtained manually using the MMP technique initially. An architecture has been designed and developed for the model and the functional analysis has been performed using VHDL. It has been observed that a complete match exists between the manual calculation of defuzzified values and the values calculated by using the proposed architecture. This shows that the architecture developed is calculating the defuzzified values correctly and efficiently.

II. DEFUZZIFICATION PROCESS

The production of the fuzzification process, a fuzzy data, is inappropriate for the real time applications and needs to be converted into a crisp value. This process of conversion from the fuzzy domain to crisp domain is the defuzzification, also called as "rounding off". The defuzzification is being done by using many methods and the method followed in this work is the “max membership principle method”. This method uses the overall output or union of all individual output fuzzy sets. The different defuzzification methods used in literature [1-4] are:

1. Center of gravity method.

2. Weighted average method.

3. Mean-max membership.

4. Centre of sums.

5. Max-membership principle.

6. Center of largest area.

7. First of maxima or last of maxima.

The first four methods have done respectively in [11-14]. While in this work the fifth’s defuzzification method (Max-membership principle) is proposed, this method is simple architecture and it is near to mean-max membership method but different for mathematically and applications.

The defuzzifier block having architecture intact based the defuzzification techniques as mentioned above to extract the defuzzified or the crisp value. The crisp output value can only be used to control various processes or mechanisms. The defuzzification technique used in this work is the max membership principle. The researchers have generally designing the VLSI architecture of the MMP defuzzifier; however, in this work an efficient MMP based defuzzifier is designed and implemented. Equation (1) shows the model for the MMP based defuzzification [1-4].

The max membership principle is found:

$\mu c(z^*) \geq \mu c(Z) \quad for\ all\ z\ \in Z \ldots\ldots\ldots (1)$ In this work, we have used a model to study and realize the defuzzification architecture as shown in Figure 1.

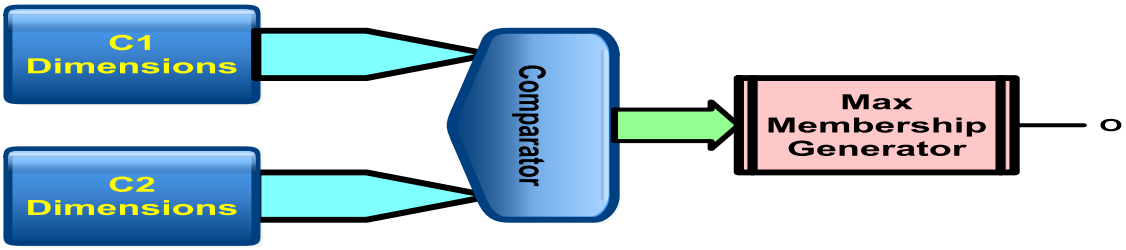

Figure 1: Block diagram of a defuzzifier.

In this model two rules are being fired and "Mamdani" implication has been used for inference. We have used aggression of rules, as the overall consequent is being obtained from the two individual consequent in each set. In each set, the minimum of two antecedent membership values is propagated to the consequent as "AND" connective is used between the two antecedents in the rule. The propagated membership value from operations on the antecedents truncates the membership function for the consequent for that rule. The truncated membership functions from each rule are aggregated according to the following equation used for conjunctive system of rules [3].

$\mu y(y) = \min\left(\mu y^1(y), \mu y^2(y), \ldots., \mu y^t(y)\right) \ldots..(2)$

$for\ y\ \in Y$

Each rule includes two antecedents (A1, B1 and A2, B2) and one consequent (C1, C2) and is represented as:

$IF\ (X\ is\ A1) AND\ (Y\ is\ B1) then\ (Z\ is\ C1) \ldots\ldots..(3)$

$IF\ (X\ is\ A2) AND\ (Y\ is\ B2) then\ (Z\ is\ C2) \ldots\ldots..(4)$

in MODEL 1, as shown in Figure 2.

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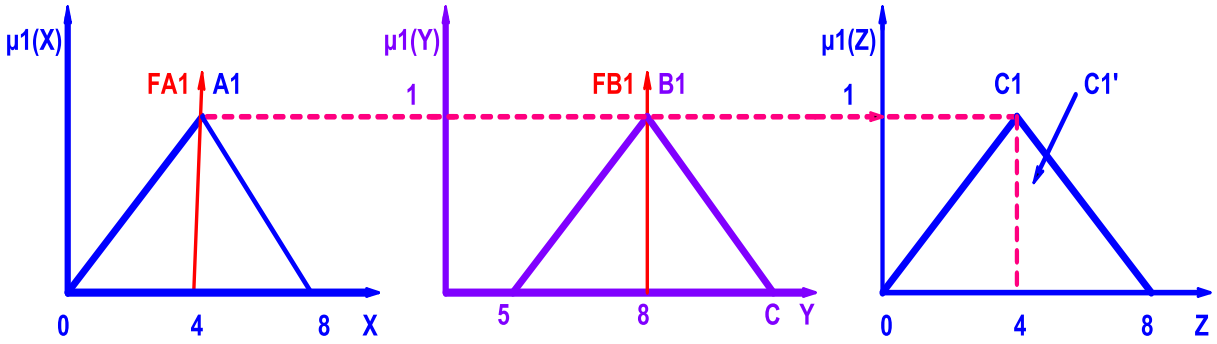
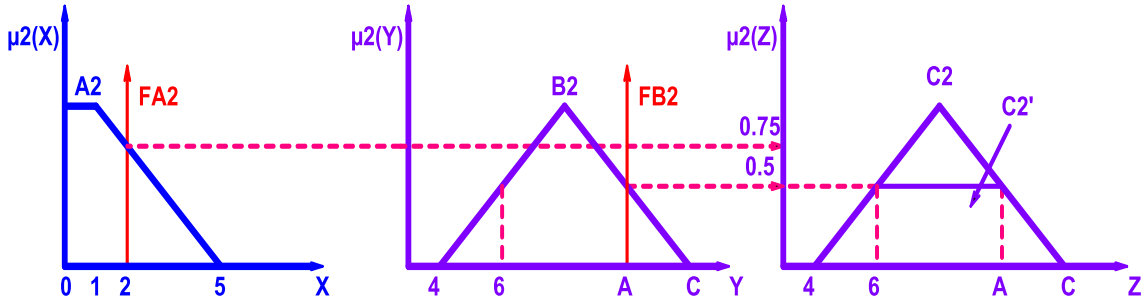
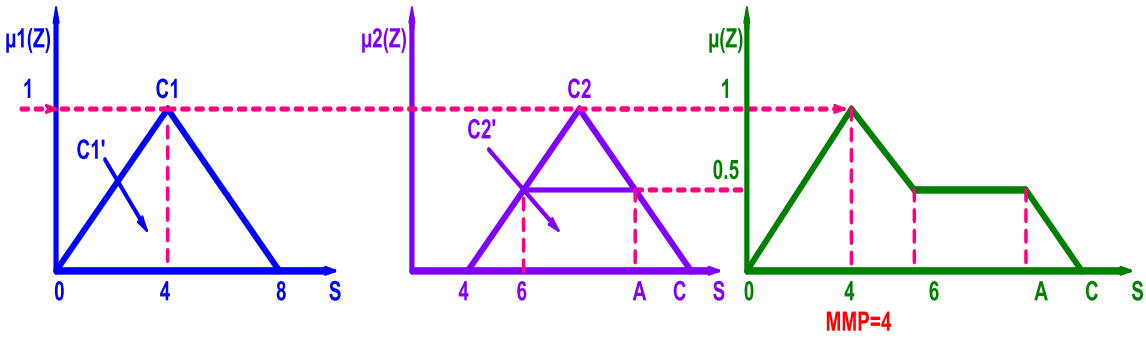
Model (1):



(a) Generator C1



(b) Generator C2



(c) Union C1 & C2

Figure 2: Fuzzification, Inference and Defuzzification using max membership principle for MODEL 1

FA1 and FB1 are the first and second fuzzy antecedents of the first rule, respectively, and C1 refers to the fuzzy consequent of that fuzzy rule. Since; the antecedents are connected by logical "AND", therefore, the minimum membership value of the antecedents propagate through to the consequent and truncates the membership function for the consequent of each rule. Similarly, FA2 and FB2 are the first and second fuzzy antecedents of the second rule, respectively, and C2 refers to the fuzzy consequent of the second fuzzy rule. This process is the inference and it follows "Mamdani's" implication method, which is the most common in practice and in the literature. The union of two consequents C1 and C2 is shown in row 3 of Figure 2. From this union the defuzzified value is being obtained by using the max membership principle (MMP) technique, as given in equation (1).

III. CALCULATION OF DEFUZZIFIED VALUES

The defuzzified or crisp value for MODEL 1 can be calculated first manually and then using the proposed architecture. It is important that the two values must match; otherwise the proposed architecture is not well designed. In this study, max membership principle (MMP) is being used to calculate the defuzzified value. Figure 3 shows the defuzzification for the MODEL 1 as given by Figure 2.

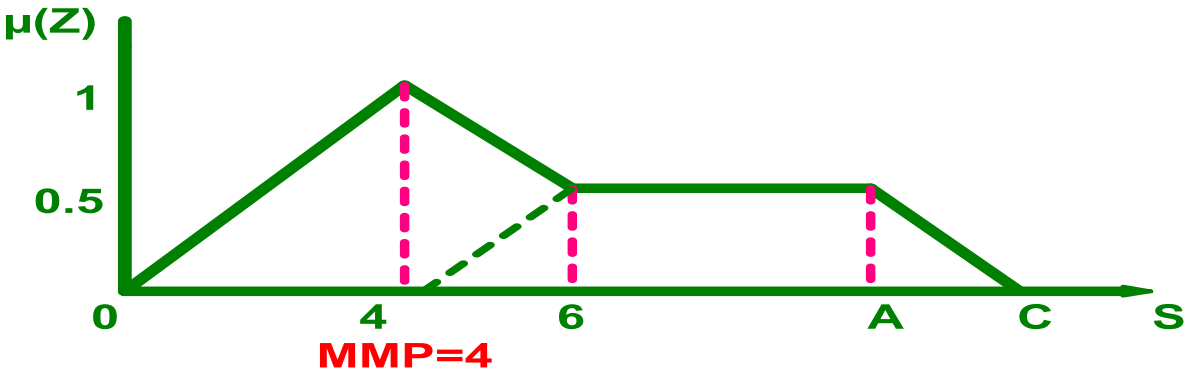


Figure 3: Defuzzification for MODEL 1

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Steps of finding MAX membership principle MMP

1- Depend on the mathematical model of the proposed architecture.

$$\mu c(z^*) \geq \mu c(Z) \quad for\ all\ z \in Z \ldots\ldots\ldots (1)$$

2- Make the comparison between Firing 1(F1) and firing 2 (F2).

3- Depending on the result got from 2, find which one has the higher values (C1 or C2).

4- Find the maximum point from the higher values got from 3.

The application of equation (1) on Figure 3 will generate the defuzzified value of model 1. The defuzzified value obtained out of MMP defuzzifier. From Equation (1), the calculations go as follows:

$$F1 = 1 = 14H, F2 = 0.5 = AH, T1 = 0,$$

The calculations have shown that the final crisp value as AH. The calculations go as follows:

$$F1 = 0.25 = 5H, F2 = 1 = 14H, T1 = 1.$$

$$T1 = 0\ (IF\ F1 > F2) \& T1 = 1\ (IF\ F1 < F2).$$

T1 control of the output of C (C1 or C2) depends of which one of higher values point from other.

$$C1X1 = 0, C2X1 = 6, CX1 = 6$$

$$T1 = 0\ (IF\ F1 > F2) \& T1 = 1\ (IF\ F1 < F2)$$

T1 control the output of C (C1 or C2) that depends on which one of higher values point from other.

$$C1X1 = 0, C2X1 = 4, CX1 = 0,$$

$$C1X2 = 8, C2X2 = C, Cx2 = 8.$$

We select C1X1 and C1X2, because; C1 is higher values point from C2, for this reason:

$$CX1 = 0, CX2 = 8.$$

$$R3 = CX1 + CX2 = 0 + 8 = 8H.$$

$$O = \frac{R3}{2} = \frac{8}{2} = 4.$$

Therefore, 4H is the manually calculated defuzzified value. Another model of type in Figure 2 has been designed and tested. The final defuzzification diagram of that model (model2) is given in Figure 4. Once more, MMP is used to calculate the defuzzified

$$C1X2 = 8, C2X2 = 14, CX2 = 14$$

We select C2X1 and C2X2, because; C2 is higher values point from C1, for this reason:

$$CX1 = 6, CX2 = 14$$

$$R3 = CX1 + CX2 = 6 + 14 = 20$$

$$O = \frac{R3}{2} = \frac{20}{2} = 10$$

The same procedure has been used for other defuzzified model3, not shown in a figure. The defuzzified value obtained is 5H.

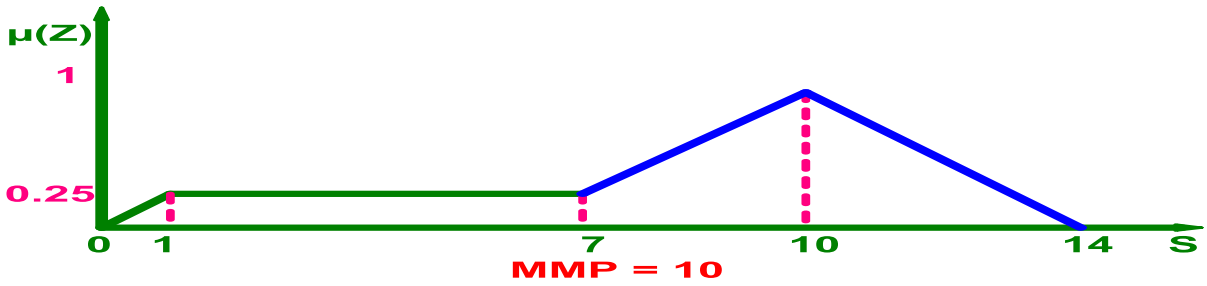

Figure 4: Defuzzification for MODEL 2

IV. Hardware realization of the defuzzification process

In the previous section, we calculated the defuzzified values manually using the MMP method. However, we need a real hardware/architecture which will automatically calculate the defuzzified values based on max membership principle technique. The defuzzified output in the MMP method is given by equation (1). It is not easy to have the hardware realization of the above equation. Equation (1) can be rewritten as to develop the architecture for the defuzzification process based on MMP, let us consider the defuzzification for the MODEL 1, as given below in Figure 3. To calculate the defuzzified value for Figure 3, we need to apply equation 1.

In section III, the defuzzified values have been manually calculated using the max membership principle, as shown in Figure 3 and Figure 4. However, manual calculation is not sufficient, a real hardware is needed which will automatically calculate the defuzzified values.

Therefore, in this section, VLSI architecture of a defuzzifier based on M.M.P. technique has been designed and simulated.

The proposed architecture has been modeled in VHDL and has been implemented in field programmable gate array (FPGA). The defuzzified output in the M.M.P is given by the equation (1).

Figure 5 is the architecture realization of the proposed architecture of equation (1).

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The VHDL modeling of the proposed architectures have been performed. The functional analysis is shown in Figure 6. It is clear from the functional analysis that there is a clear cut match between the results generated by the architecture and the results obtained manually.

In the first T-state of the functional analysis, the output of the defuzzifier 'O' is 4H, which is same as obtained manually for Model 1. Similarly, for T-State second and third, the outputs of the defuzzifier is AH and 5H respectively, which is same as calculated manually. This shows the proposed architecture is realizing the defuzzifier action efficiently and accurately.

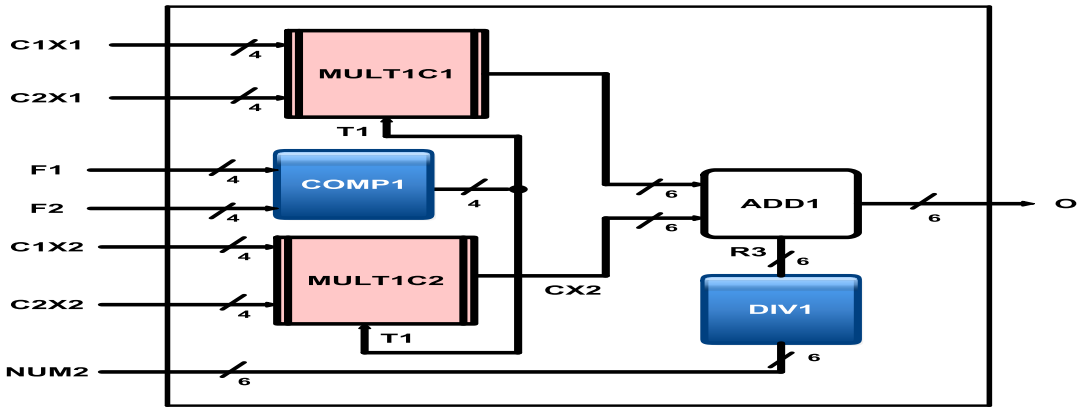

Figure 5: Proposed Architecture of the defuzzifier.

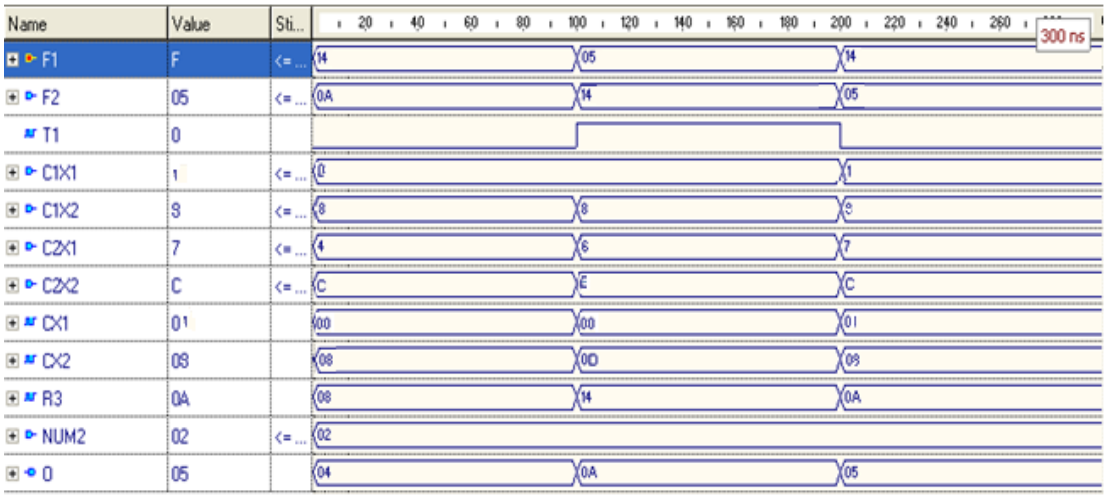

Figure 6: Timing diagram of the proposed defuzzifier

V. FPGA IMPLEMENTATION OF THE DEFUZZIFIER

A Spartan 3E (XC3S100E - 5vq100) FPGA platform from XILINX has been used to implement the proposed architecture. The FPGA has around 1920 4-input look up tables (LUT) and 66 bonded input/output buffers (IOB). The FPGA logic resource used in an implementation are shown in Table 1:

TABLE 1: FPGA Implementation results

Device Utilization Summary (FPGA: Spartan 3E XC3S100E)		
Logic Utilization	**Used**	**Available**
Number of 4 input LUTs	11	1,920
Number of occupied Slices	6	960
Number of Slices containing only related logic	6	6
Number of Slices containing unrelated logic	0	6
Total Number of 4 input LUTs	11	1,920
Number of bonded IOBs	32	66
Average Fanout of Non-Clock Nets	1.32	

While, a schematic and netlist generated of the proposed defuzzifier shown in Figure7 and 8 respectively. The implementation results shown in Table 1 show that that there is further scope for improvement in the proposed structures by incorporeity more parallelism in the architecture.

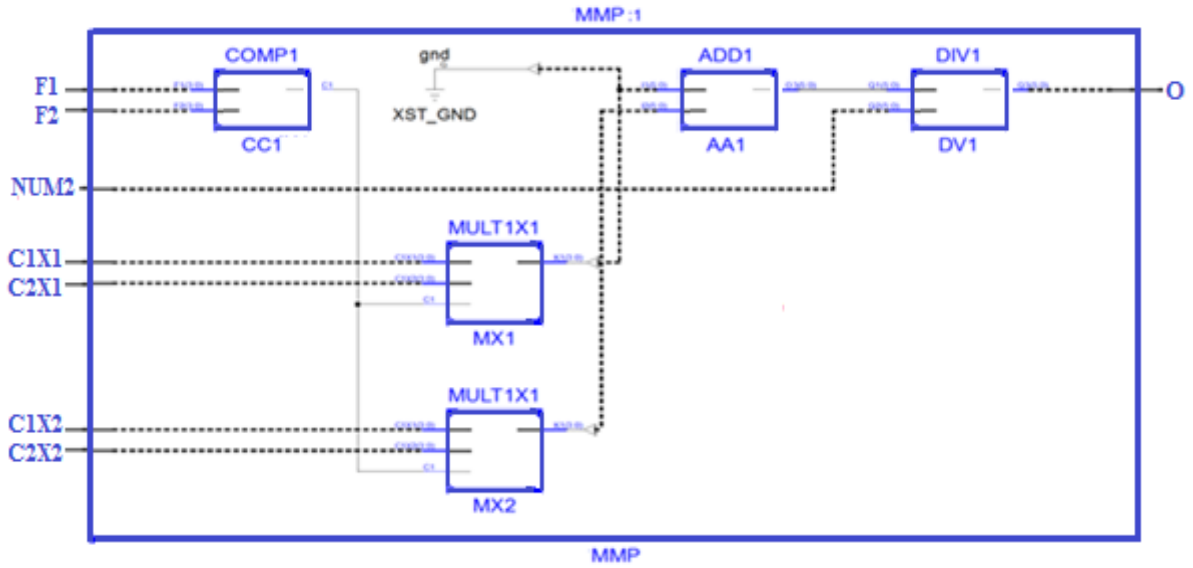

Figure 7: Schematic of the proposed Architecture

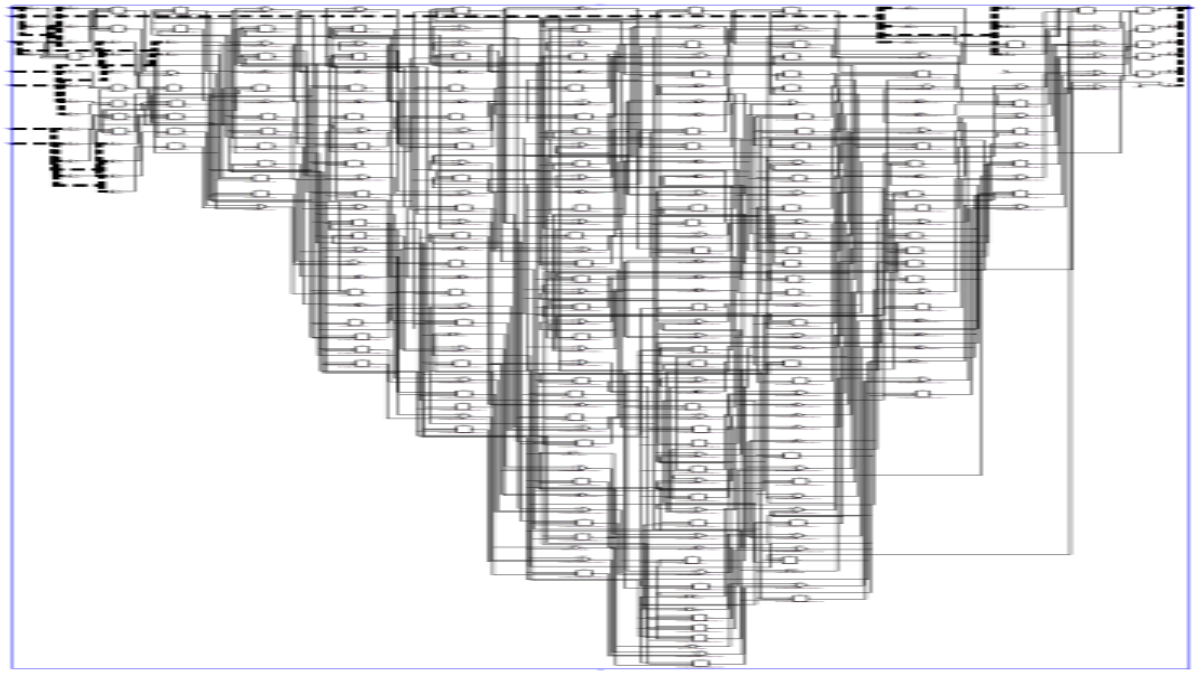

Figure 8: Netlist generated by the synthesis tools.

CONCLUSION

In this paper, VLSI architecture of a defuzzifier is proposed. The Max Membership Principle MMP which considered as the most important and simplest way of the defuzzification methods is used. Initially, the defuzzified values have been manually calculated and finally obtained by the proposed architecture.

Then the VHDL modeling and Spartan-3 FPGA implementation has been done. Finally, it has been gotten that the proposed architecture recognizes MMP based defuzzifier efficiently, as well as there is an ample match between the results obtained manually and through the architecture.

REFERENCES

[1] L. A. Zadeh, "Fuzzy sets", Information and Control, Vol. 8, pp. 338- 351, (1965).

[2] T. J. Ross, "fuzzy logic with engineering applications," by John Wiley Sons inc., (2005).

[3] E. H. Mamdani, "Applications of fuzzy algorithm for simple dynamic plant", Proc. Inst. Elect. Eng., Vol. 121, pp. 1585-1588, (1974).

[4] C. C. Lee, "Fuzzy logic in control systems: fuzzy logic controller-part I", IEEE Trans. Syst., Man. Cybern., Vol. 20, no. 2, pp. 404-418, (1990).

[5] A. M. Murshid, S. A. Loan, S. A. Abbasi, and A. M. Alamoud, "VLSI Architecture of Fuzzy Logic Hardware Implementation: a Review," Int. Journal of Fuzzy Systems, Vol. 13, No. 2, pp. 74-88, June (2011).

[6] H. Watanabe, W. D. Dettloff, and K. E. Yount, "A VLSI fuzzy logic Controller with reconfigurable, cascade architecture", IEEE Journal of Solid-State Circuits, Vol. 25, pp. 376-381, (1990).

[7] M. Togai and H. Watanabe, "Expert system on a chip: an engine for real-Time approximate reasoning", IEEE Expert Mag., Vol. 1, pp. 55- 62, (1986).

[8] H. Peyravi, A. Khoei, and K. Hadidi, "Design of an analog CMOS fuzzy logic controller chip", Fuzzy Sets and Systems 132, PP. 254- 260, 2002.

[9] J. M. Jou and P. Y. Chen", "An adaptive fuzzy logic controller: its VLSI architecture and applications", IEEE Trans. Very Large Scale Integration (VLSI) Systems, Vol. 8, pp. 52-60, (2000).

[10] N. E. Evmorfopoulos, and J. N. Avaritsiots, "An adaptive digital fuzzy architecture for application-specific integrated circuits", Active and Passive Elec. Comp., Vol. 25, pp. 289-306, (2002).

[11] Sajad A. Loan, Asim M. Murshid and Faisal Bashir, "A Novel VLSI Architecture of a Defuzzifier Unit for a fuzzy Inference processor", in proceeding of IEEE International Conference Of Advanced Electronic Systems, India, Pilani, 21-23, September, (2013).

[12] Sajad A. Loan, Asim M. Murshid and Ahmed C. Shakir, "A Novel VLSI Architecture of a Weighted Average Method based Defuzzifier Unit", in proceeding of IAENG International Multi Conference of Engineers and Computer Scientists, Hong Kong, 12-14, March, (2014).

[13] Asim M. Murshid, "FPGA Implementation of Mean – Max Membership based Defuzzifier Unit", Kirkuk University Journal/Scientific Studies (KUJSS), Vol.10, Isuue 3, pp. 79-91, Sep. (2015).

[14] Asim M. Mursid, "Center of Sums based Defuzzifier Unit VLSI Architecture", Tikrit Journal of Pure Science,Vol.21, No. 1, pp. 87-94, Jan. (2016).

[15] S. A. Loan, A. M. Murshid, S. A. Abbasi, and A. M. Alamoud,"A Novel Multi Membership Function Based VLSI Architecture of a Fuzzy Inference Processor", Springer - International journal of Fuzzy Systems, Vol. 16, No. 4, pp. 468-482, Dec. (2014).

معمارية الدوائر المتكاملة ذات الكثافة العالية جداً لمبدأ أقصى قيمة بالاعتماد على وحدة فك الغامض

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المستخلص :

البيانات الغامضة الناتجة من عملية الغموض ليست مناسبة للتطبيقات في الوقت الحقيقي فإنه لا بد من تحويلها إلى قيمة واضحة. تحويل البيانات من الغامض إلى قيمة واضحة تسمى فك الغامض كذلك تسمى "التقريب". هذا البحث يقترح معمارية دوائر متكاملة ذات الكثافة العالية جداً لمبدأ أقصى قيمة كطريقة فك الغامض. طريقة مبدأ أقصى قيمة لفك الغامض بسيطة ويستخدم عموماً بالمقارنة مع طرق أكثر تعقيداً كطريقة متوسط الوزن لفك الغامض. تم كتابة وتنفيذ كودات البرنامج بطريقة تنفيذ الدوائر الالكترونية عالية الدقة المعروفة (VHDL) وتنفيذها على (XILINX) والجهاز المستخدم لهذا الغرض (Spartan-3) في مجموعة بوابة حقل برنامج (FPGA). المعمارية المقترحة هو أكثر كفاءة في المساحة وسرعة العملية بالمقارنة مع معمارية أكثر تعقيداً المستخدمة في طريقة متوسط الوزن. وقد كشف التحليل الوظيفي أن المعمارية المقترحة بتنفيذ FMLM لفك الضبابية ذات كفاءة ودقة.