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The Rational Selection of the Modules of the Values for the Processors in the System of the Residual Classes

Rusul Jabbar Alsaedi [a]

[a] *Al-Qasim University - Al-Qasim - Babylon – Iraq* , Email*: rusul@uoqasim.edu.iq*

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ABSTRACT

Considered there is a set of systems of modules for 32-bit and 64-bit processors in the residual number system (RNS). The conducted substantiation of the selection criteria of values of the modules with a minimum of hardware expenses tabular implementation of RNS processor; minimum hardware expenses in the implementation of RNS processor in the binary logic which is the same type of module channels. Considered there are various systems of modules in the amount of 25 sets for 32- bit and 22 sets for 64-bit processors. The conducted investigations determine the effectiveness of the use of all sets under the consideration systems of modules in terms of each of criteria. The present analysis of the results selected the best criteria according to the systems of modules for each of the processors.

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1. Introduction

The system of residual classes (RNS) represents the number A residues from dividing α_1, α_2, ..., α_n by mutually simple modules (bases) p_1, p_2, ..., p_n, [1]. The operation of obtaining the residue (residue) αi from the number A module pi is determined by the rule.

$$\forall A \in Z: |A|_{P_i}^{+} \leftrightarrow A\left[\frac{A}{p_i}\right]^{+} . P_i \qquad (1.1)$$

Corresponding author *Rusul Jabbar Alsaedi*

Email address: *rusul@uoqasim.edu.iq*

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Where Z- is the set of integers;

[·] - The operation of integer division

The residual α_i module p_i is a number in the interval $[\overline{0, p_i - 1}]$. As a result of such a presentation, the processor operates with low-bit residues processed by parallel modular computational channels. RNS, having the maximum level of internal parallelism, increases the speed of performing arithmetic operations and ensures the independence of parallel processing on the basis of the number system modules, which ultimately leads to a significant increase in the processor performance.

The range of numbers representable in the RNS is determined by the product of mutually simple bases $P = p_1. p_2 ... p_n$. Therefore, to overlap the required range of P, one should choose such a set of bases, the product which is equal to or slightly higher than the value of R. The modern processors operating in the positional number system have a capacity multiple of power 2, usually 32 or 64 bits. The range of representation of numbers that they overlap is respectively $P = 2^{32} \approx 4.29 \times 10^9 = 4.29\ E + 9$, $P_{64} = 2^{64} \approx 1.84 \times 10^{19} = 1.84\ E + 19$.

In [2], they did more study on the experimental design and analysis by studying the big picture of the importance of careful experimental design and the statistical analysis. In [3], they studied how to setup the satellite and aerial photography projects, how to compute the math model, DEM operations, and mosaicking.

In our studies, we will rely on the given values of the ranges of representation of numbers since the main role of computing devices in the RNS is to perform the functions of coprocessors to the positional processors in those operations and functions that give a significant gain in speed over the positional number system [1]. Modern studies do not address the issues of choosing a set of modules for the processors operating in the RNS. In [4], the values of the sets of modules for actually developed in the 60–70s of the last century computers T-340A, K-340A, *Almaz*, 5E53 are given, but it does not say what justified the choice of these modules. In a number of articles, for example [5], Modules of a special type $\{2^n\text{-}1, 2^2, 2^{n+1}\}$ are analyzed, which have advantages in performing modular operations in comparison with arbitrary sets of mutually simple bases, but, as a rule, three modules are not enough to simultaneously overlap large number representation ranges and fault tolerance of the RNS processor [6]. In this article, the authors propose their own vision of the question of justifying the choice of module values for 32-x and 64-x processors operating in the RNS.

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Cfurther nomenclature continues down the page inside the text box

2. The Materials and Methods of Research

Let us consider possible approaches to the determination and selection of the values of modules RNS separately for 32-x and 64-x processors since significantly the different ranges of representation of numbers can make their own adjustments to the choice of grounds for the system of residual classes.

2.1.For 32-X Processor

To perform arithmetic operations on numbers in the 32-bit binary range, it is necessary to select mutually simple numbers (RNS modules); the product of which would overlap the number representation range $2^{32} \approx 4.29 \times 10^9 = 4.29E + 9$. However, the choice of arbitrary modules will not always meet the requirement of minimization of hardware costs and manufacturability of the design of modular channels. In a connection with the foregoing, we make a selection of modules and analysis of the resulting system of residual classes according to the following criteria.

1. The minimum hardware costs for the table implementation of the processor RNS. This criterion is estimated by the total bit depth of the selected RNS bases in the tabular organization of calculations [4, 6].

2. The minimum of hardware costs when implementing the RNS processor in the binary logic. This criterion is estimated by the total bit depth of the selected bases of the RNS when they are represented in the binary number system.

3. The uniformity of modular channels. The evaluation of this criterion is carried out by comparing the smallest and the greatest bit depth of the modules that make up the base system. The smaller the differences in the capacity of the modules, the more technological of the same type will be the implementation of the modular channels [7].

The choice of bases was carried out in such a way that it was possible to uniquely encode any number in the range $2^{32} \approx 4.29 \times 10^9 = 4.29E + 9$. That is the product of the values of the modules that should not be less than this range, and if it is possible, minimally exceed it. A significant excess of the range of 2^{32} leads to a significant increase in the hardware costs. The base systems for the 32-bit range are presented in Table 1, which contains 25 base sets [8]. The first set was composed in ascending order of mutually simple numbers, starting with the number 2. The second set and further were selected according to the following algorithm; the smallest base is removed, and if the set stops covering the required range, a new base is added that exceeds the last base by the minimum value. The general requirement for such a selection was the mutual simplicity of the base system. The results of this simulation are

Corresponding author : *Rusul Jabbar Alsaedi*

Email address: *rusul@uoqasim.edu.iq*

Communicated by : *Alaa Hussein Hamadi*

presented in table 1. Here, the columns corresponding to the RNS modules $p_1, p_2, ..., p_{10}$ represent the vary base and the bit of its implementation in the binary notation (the number in brackets). The width of the table implementation is determined by the sum of the values of the bases themselves [6], and the bit depth of the binary implementation is determined by the sum of the width of the bases in the binary number system (the numbers in brackets), for all bases sets (Fig. 1–3).

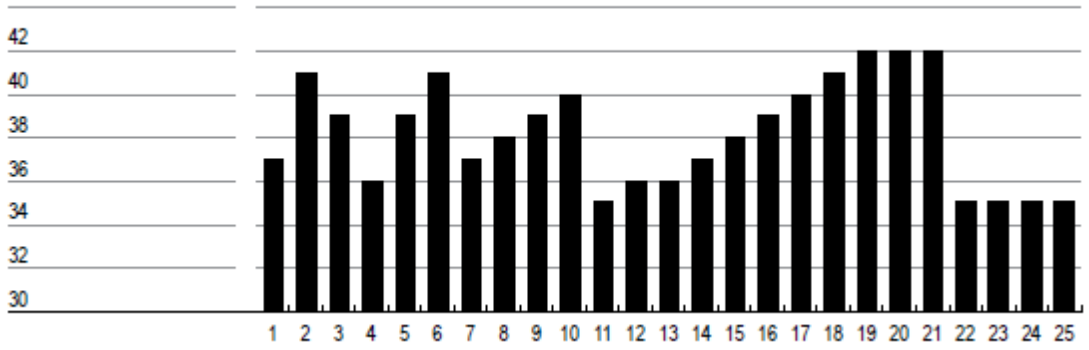

Fig. 1- diagram of the table implementation.

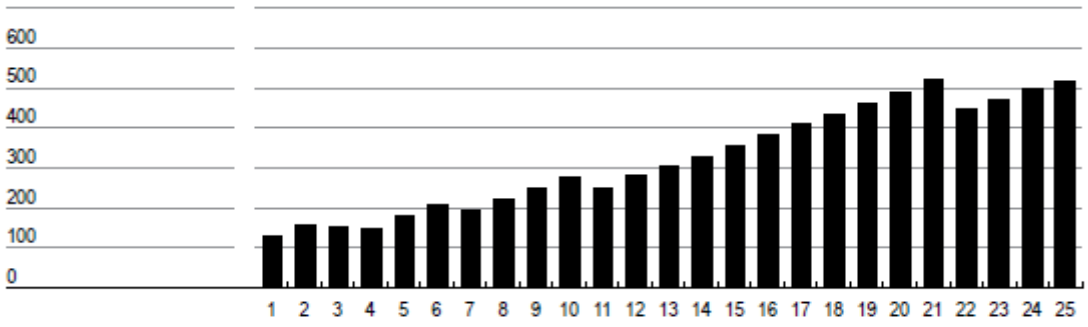

Fig. 2 - diagram of the binary implementation.

Table 1 - Jacket Basis Systems for Range 2^{32}

Dial Number	p_1	p_2	p_3	p_4	p_5	p_6	p_7	p_8	p_9	p_{10}	Digit size in the table imnlementatio	Digit in binary implementati	Encoding range
1.	2(1)	3(2)	5(3)	7(3)	11(4)	13(4)	17(5)	19(5)	23(5)	29(5)	129	37	6,47E+09
2.	3(2)	5(3)	7(3)	11(4)	13(4)	17(5)	19(5)	23(5)	29(5)	31(5)	158	41	1E+11
3.	5(3)	7(3)	11(4)	13(4)	17(5)	19(5)	23(5)	29(5)	31(5)		155	39	3,34E+10
4.	7(3)	11(4)	13(4)	17(5)	19(5)	23(5)	29(5)	31(5)			150	36	6,69E+09
5.	11(4)	13(4)	17(5)	19(5)	23(5)	29(5)	31(5)	37(6)			180	39	3,53E+10

6.	13(4)	17(5)	19(5)	23(5)	29(5)	31(5)	37(6)	41(6)	210	41	1,32E+11
7.	17(5)	19(5)	23(5)	29(5)	31(5)	37(6)	41(6)		197	37	1,01E+10
8.	19(5)	23(5)	29(5)	31(5)	37(6)	41(6)	43(6)		223	38	2,56E+10
9.	23(5)	29(5)	31(5)	37(6)	41(6)	43(6)	47(6)		251	39	6,34E+10
10.	29(5)	31(5)	37(6)	41(6)	43(6)	47(6)	53(6)		281	40	1,46E+11
11.	31(5)	37(6)	41(6)	43(6)	47(6)	53(6)			252	35	5,04E+09
12.	37(6)	41(6)	43(6)	47(6)	53(6)	59(6)			280	36	9,59E+09
13.	41(6)	43(6)	47(6)	53(6)	59(6)	61(6)			304	36	1,58E+10
14.	43(6)	47(6)	53(6)	59(6)	61(6)	67(7)			330	37	2,58E+10
15.	47(6)	53(6)	59(6)	61(6)	67(7)	71(7)			358	38	4,26E+10
16.	53(6)	59(6)	61(6)	67(7)	71(7)	73(7)			384	39	6,62E+10
17.	59(7)	61(7)	67(7)	71(7)	73(7)	79(7)			410	40	9,87E+10
18.	61(6)	67(7)	71(7)	73(7)	79(7)	83(7)			434	41	1,39E+11
19.	67(7)	71(7)	73(7)	79(7)	83(7)	89(7)			462	42	2,03E+11
20.	71(7)	73(7)	79(7)	83(7)	89(7)	97(7)			492	42	2,93E+11
21.	73(7)	79(7)	83(7)	89(7)	97(7)	101(7)			522	42	4,17E+11
22.	79(7)	83(7)	89(7)	97(7)	101(7)				449	35	5,72E+09
23.	83(7)	89(7)	97(7)	101(7)	103(7)				473	35	7,45E+09
24.	89(7)	97(7) 107(7)	101(7)	103(7)	497					35	9,61E+09
25.	97(7)	101(7) 109(7)	103(7)	107(7)	517					35	1,18E+10

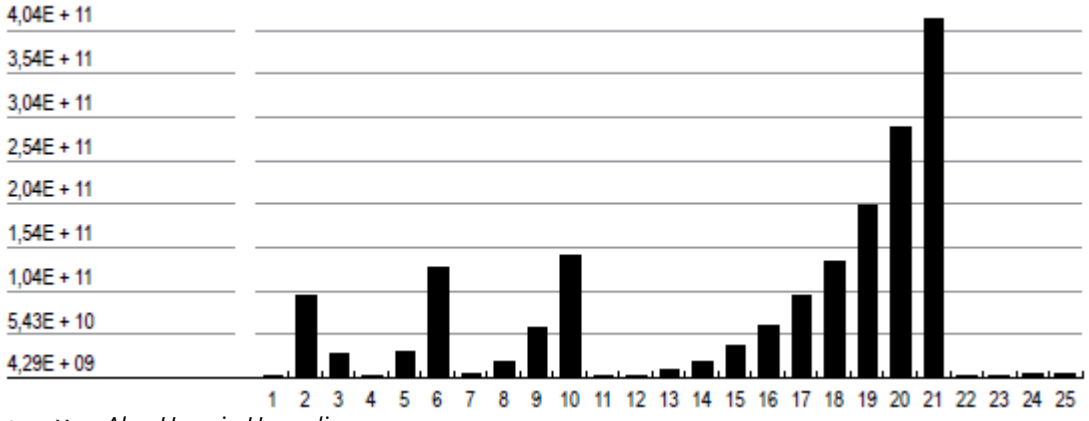

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Fig. 3 - chart of the value of the coded range.

2.2. For 64-X Processor

The study focuses on the base systems of overlapping; the range is 264 ≈ 1.84 × 1019 = 1.84E + 19. The approach for determining the values of the bases will be the same as for the 32-bit processor with some limitation of the size of the base. The choice of the base is limited to 127, so that the binary implementation of the modular channel does not exceed 7 bits. As a result, 22 sets of the base systems are presented, which are presented in Table 2. We present similar diagrams of the tabular and binary implementation; as well as, the values of the coded range for all base sets (Fig. 4-6).

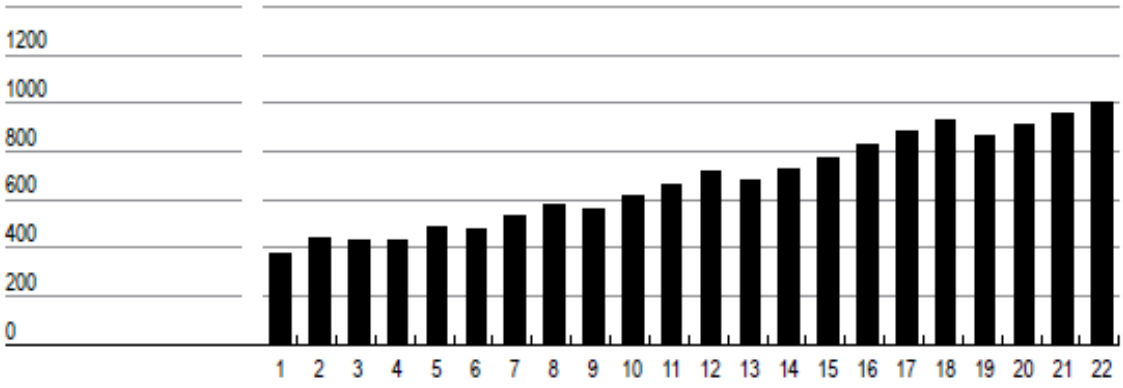

Fig. 4 - diagram of the table implementation.

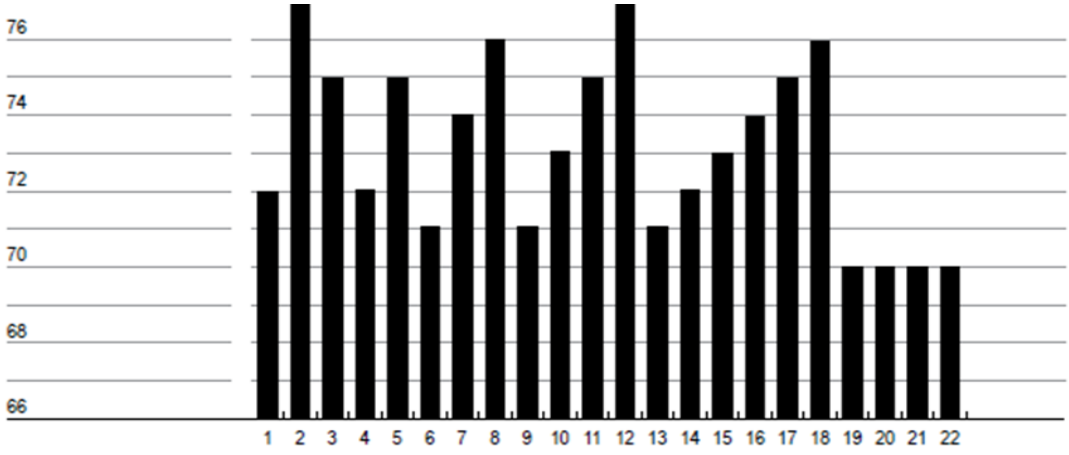

Fig. 5 - diagram of the binary implementation.

Table 2 - Jacket Basis Systems for Range 2^{64}

p_1	p_2	p_3	p_4	p_5	p_6	p_7	p_8	p_9	p_{10}	p_{11}	p_{12}	p_{13}	p_{14}	p_{15}	p_{16}	Tabular implementation	Binary implementation	Encoding range
2	3	5	7	11	13	17	19	23	29	31	37	41	43	47	53	381	72	3.2589E+19
3	5	7	11	13	17	19	23	29	31	37	41	43	47	53	59	438	77	9.6138E+20
5	7	11	13	17	19	23	29	31	37	41	43	47	53	59		435	75	3.2046E+20
7	11	13	17	19	23	29	31	37	41	43	47	53	59			430	72	6.4092E+19
11	13	17	19	23	29	31	37	41	43	47	53	59	61			484	75	5.5852E+20
13	17	19	23	29	31	37	41	43	47	53	59	61				473	71	5.0774E+19
17	19	23	29	31	37	41	43	47	53	59	61	67				527	74	2.6168E+20
19	23	29	31	37	41	43	47	53	59	61	67	71				581	76	1.0929E+21
23	29	31	37	41	43	47	53	59	61	67	71					562	71	5.7522E+19
29	31	37	41	43	47	53	59	61	67	71	73					612	73	1.8257E+20
31	37	41	43	47	53	59	61	67	71	73	79					662	75	4.9734E+20
37	41	43	47	53	59	61	67	71	73	79	83					714	77	1.3316E+21
41	43	47	53	59	61	67	71	73	79	83						677	71	3.5989E+19
43	47	53	59	61	67	71	73	79	83	89						725	72	7.8122E+19
47	53	59	61	67	71	73	79	83	89	97						779	73	1.7623E+20

Corresponding author : *Rusul Jabbar Alsaedi*

Email address: *rusul@uoqasim.edu.iq*

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53	59	61	67	71	73	79	83	89	97	101	833	74	3.7871E+20
59	61	67	71	73	79	83	89	97	101	103	883	75	7.3598E+20
61	67	71	73	79	83	89	97	101	103	107	931	76	1.3347E+21
67	71	73	79	83	89	97	101	103	107		870	70	2.1881E+19
71	73	79	83	89	97	101	103	107	109		912	70	3.5597E+19
73	79	83	89	97	101	103	107	109	113		954	70	5.6655E+19

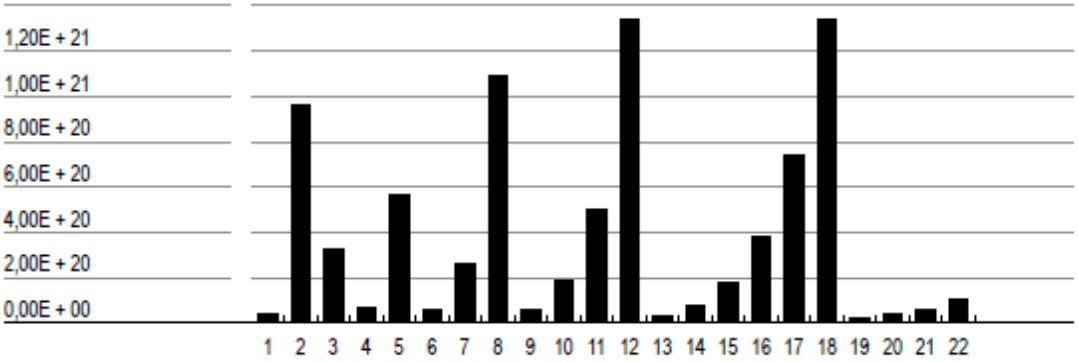

Fig. 6 - diagram of the value of the coded range.

3. Results of Research

3.1. 32-X Processor

From the diagram of the digitization of the table implementation (Fig. 1), it follows that in the most cases of an increase in the values of the RNS modules, the total costs of implementing the processor increase. At the same time, there are separate systems of bases, such as under the numbers 3, 4, 7, 11, 22, and 23 in Table 1, which are less expensive than the systems preceding them in the table, but despite of these facts, the lowest cost for a table implementation will be provided by the base system 1, which was selected in a sequential increase in the bases, starting with *p1 = 2*. The costs of implementing modular channels in the binary number system (Fig. 2) are not so dependent on the increase in the values of the modules; on the contrary, the lowest costs are observed for base systems 22–25, where the magnitude of the RNS modules is the greatest. The same costs are for the base system 11.

The analysis of the coded range (Fig. 3) shows that the largest deviation from the required range of $2^{32} \approx 1.29 \cdot 10^9$ is observed for the base systems 2, 6, 10, and 18–21. The same base systems require the largest hardware costs for both binary and tabular implementation of the RNS system. From this, we can conclude that the chosen base system will be less costly if its overlapping operating range only slightly exceeds the coded range of numbers. From the point of view of uniformity and the technological design of the modular channels, the best base systems are those that, when implemented in the binary number system, have the same number of digits. These are systems 12, 13, and 19–25. However, systems 19–21 require large hardware expenditures for both the binary and tabular

implementations; hence, their use in the ROS processor is inexpedient. The systems of the bases that satisfy all three criteria described above are systems 12 and 13. These are sets of bases {37, 41, 43, 47, 53, 59} and {41, 43, 47, 53, 59, 61}.

3.2. 64-X Processor

From the diagram of the digit capacity of the table implementation (Fig.4), the best base systems in terms of the minimum hardware costs are the first four systems; as well as, 6, 9, 13, and 19, which are less expensive than the preceding number systems. However, the lowest cost for the table implementation is required by the base system 1, which was selected in a sequential increase in the bases, starting with *p1 = 2*. When the modular channels are implemented in the binary number system (Fig. 5), the lowest costs are observed for the base systems 19–21, where the magnitude of the RNS modules is the highest. The results of the analysis of the value of the coded range (Fig. 6) state that the greatest deviation from the required range of $2^{64} \approx 1.84 \times 10^{19}$ is observed for the base systems 2, 5, 8, 12, and 18. These same base systems require the greatest hardware costs for tabular and especially the binary implementation of the RNS processor. From the point of view of uniformity and the technological design of the modular channels, the best base systems are systems 19-22, which, when implemented in a binary number system, have the same number of the digits equal to 7. These same base systems require the least hardware when implementing a processor in the binary number system. They have insignificant deviations from the coded range of $2^{64} \approx 1.84 \times 10^{19}$. However, these systems, when implemented in the tabular form, are expensive. Therefore, they should be recommended for the binary implementation of the processor and the best base system from the sets 19–22 is the set 19 - {67, 71, 73, 79, 83, 89, 97, 101, 103, 107}. For the table implementation, you can recommend the sets of 1, 4, and 6 that satisfy the requirements of minimizing hardware costs and the slight deviation from the range of representation of the numbers 2^{64}. The system of the bases that most fully meets all three criteria described above should include the system 13 - {41, 43, 47, 53, 59, 61, 67, 71, 73, 79, 83}, but since the RNS processor can be the hardware implemented either in the binary number system or in the tabular form, it is necessary to select the system of the modules separately for each implementation.

4. Conclusion

The proposed approach to justify the choice of the module values for the RNS processors, based on the criteria for minimizing hardware costs and the uniformity of the implementation of the modular channels, is one of the options for the scientific approach to solve this problem. It will allow developers to simplify the procedure for determining the basis of the RNS and reduce the cost of implementing the processor. The subsequent studies on the

Corresponding author : *Rusul Jabbar Alsaedi*

Email address: *rusul@uoqasim.edu.iq*

Communicated by : *Alaa Hussein Hamadi*

choice of modules for the RNS processors can be aimed at substantiating and choosing the values of the control bases for the redundant system of the residual classes when constructing fault-tolerant computing devices.

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